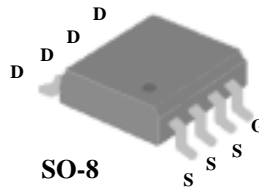


- ▼ Simple Drive Requirement
- ▼ Lower Gate Charge
- ▼ Fast Switching Characteristic

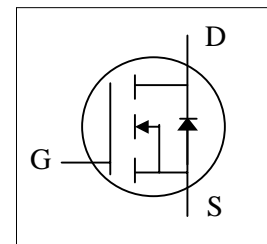


$BV_{DSS}$	80V
$R_{DS(ON)}$	45m $\Omega$
$I_D$	5.3A

## Description

The Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SO-8 package is universally preferred for all commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.



## Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	80	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D @ T_A=25^\circ\text{C}$	Continuous Drain Current <sup>3</sup>	5.3	A
$I_D @ T_A=100^\circ\text{C}$	Continuous Drain Current <sup>3</sup>	3.4	A
$I_{DM}$	Pulsed Drain Current <sup>1</sup>	50	A
$P_D @ T_A=25^\circ\text{C}$	Total Power Dissipation	2.5	W
	Linear Derating Factor	0.02	W/ $^\circ\text{C}$
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

## Thermal Data

Symbol	Parameter	Value	Unit
$R_{thj-a}$	Thermal Resistance Junction-ambient <sup>3</sup>	Max. 50	$^\circ\text{C}/\text{W}$



# AP9685M

## Electrical Characteristics @T<sub>j</sub>=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =1mA	80	-	-	V
ΔBV <sub>DSS</sub> /ΔT <sub>j</sub>	Breakdown Voltage Temperature Coefficient	Reference to 25°C, I <sub>D</sub> =1mA	-	0.073	-	V/°C
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V, I <sub>D</sub> =5.3A	-	-	45	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =3.0A	-	-	50	mΩ
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	1	-	3	V
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =10V, I <sub>D</sub> =5A	-	9	-	S
I <sub>DSS</sub>	Drain-Source Leakage Current (T <sub>j</sub> =25°C)	V <sub>DS</sub> =80V, V <sub>GS</sub> =0V	-	-	1	uA
	Drain-Source Leakage Current (T <sub>j</sub> =70°C)	V <sub>DS</sub> =64V, V <sub>GS</sub> =0V	-	-	25	uA
I <sub>GSS</sub>	Gate-Source Leakage	V <sub>GS</sub> = ± 20V	-	-	±100	nA
Q <sub>g</sub>	Total Gate Charge <sup>2</sup>	I <sub>D</sub> =5A	-	19	30	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =64V	-	5	-	nC
Q <sub>gd</sub>	Gate-Drain ("Miller") Charge	V <sub>GS</sub> =4.5V	-	10	-	nC
t <sub>d(on)</sub>	Turn-on Delay Time <sup>2</sup>	V <sub>DS</sub> =40V	-	11	-	ns
t <sub>r</sub>	Rise Time	I <sub>D</sub> =1A	-	6	-	ns
t <sub>d(off)</sub>	Turn-off Delay Time	R <sub>G</sub> =3.3Ω, V <sub>GS</sub> =10V	-	36	-	ns
t <sub>f</sub>	Fall Time	R <sub>D</sub> =40Ω	-	22	-	ns
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V	-	1710	2730	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> =25V	-	135	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	f=1.0MHz	-	98	-	pF

## Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V <sub>SD</sub>	Forward On Voltage <sup>2</sup>	I <sub>S</sub> =2A, V <sub>GS</sub> =0V	-	-	1.2	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>S</sub> =5A, V <sub>GS</sub> =0V,	-	42	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge	dI/dt=100A/μs	-	84	-	nC

### Notes:

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse width ≤300us , duty cycle ≤2%.
- 3.Surface mounted on 1 in<sup>2</sup> copper pad of FR4 board ; 125 °C/W when mounted on min. copper pad.

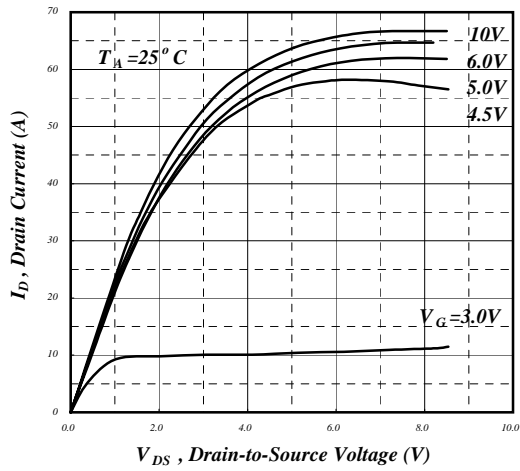


Fig 1. Typical Output Characteristics

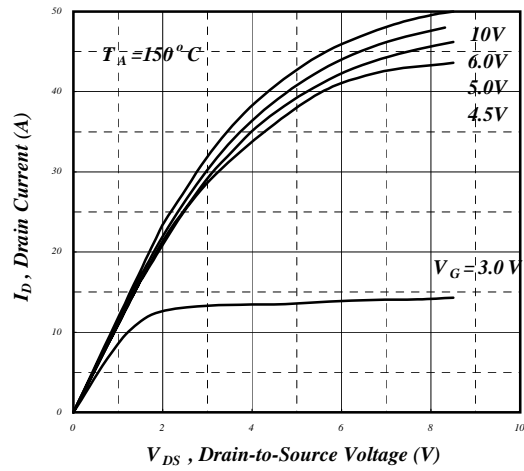


Fig 2. Typical Output Characteristics

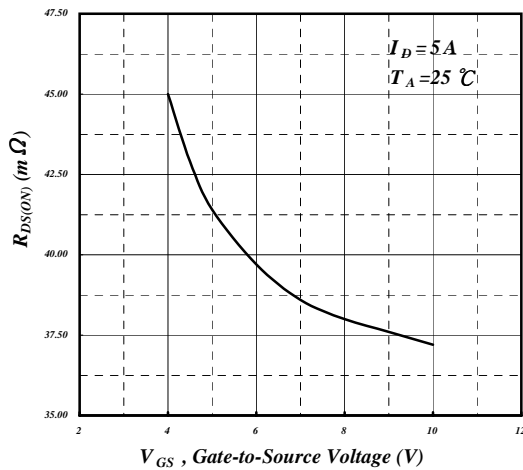


Fig 3. On-Resistance v.s. Gate Voltage

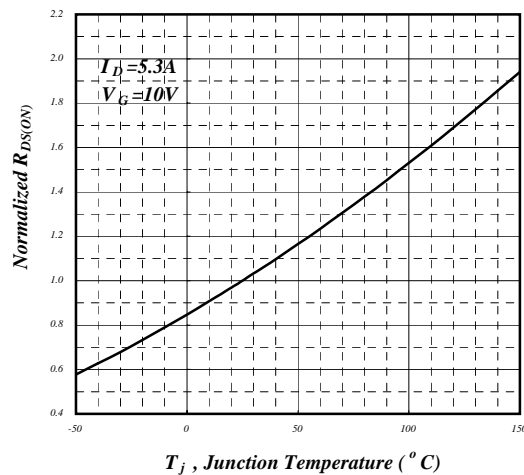


Fig 4. Normalized On-Resistance v.s. Junction Temperature

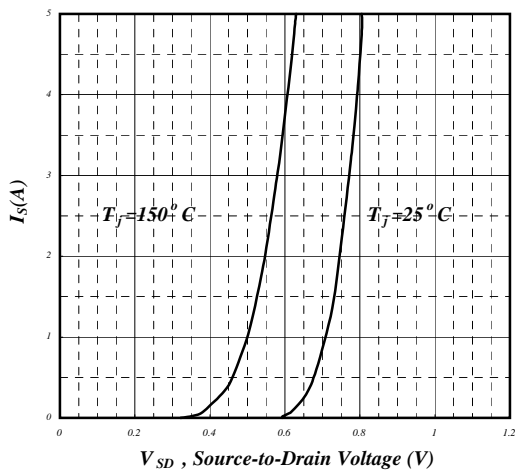


Fig 5. Forward Characteristic of Reverse Diode

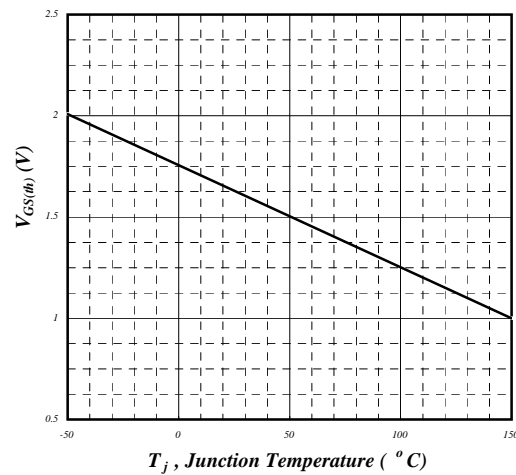


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

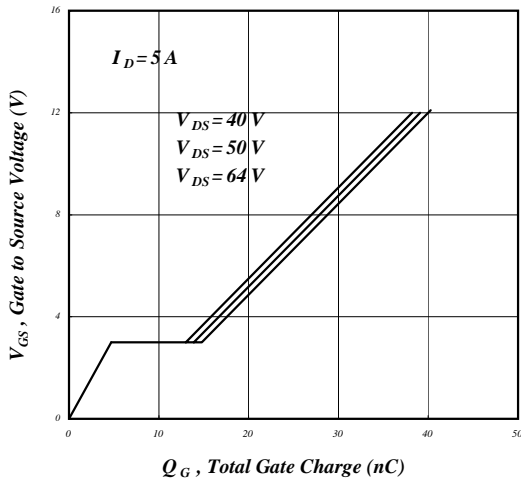


Fig 7. Gate Charge Characteristics

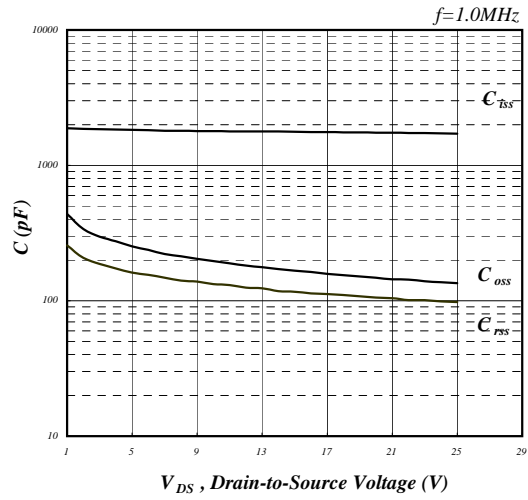


Fig 8. Typical Capacitance Characteristics

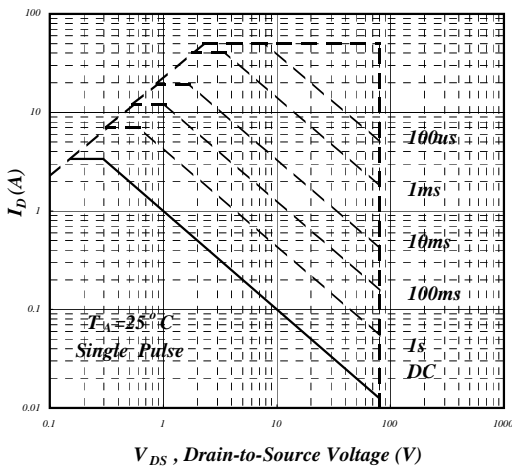


Fig 9. Maximum Safe Operating Area

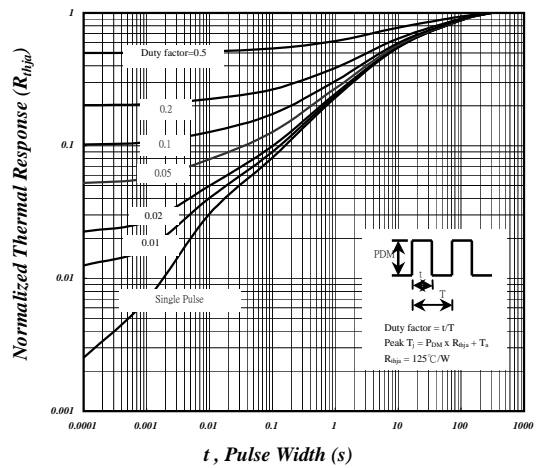


Fig 10. Effective Transient Thermal Impedance

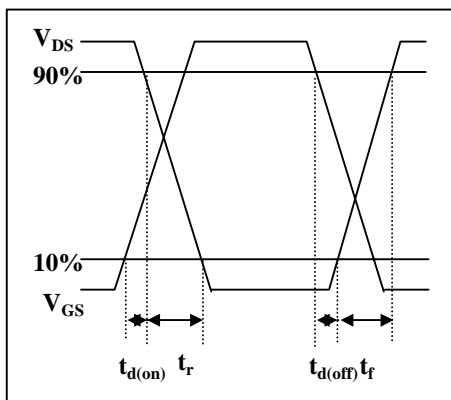


Fig 11. Switching Time Waveform

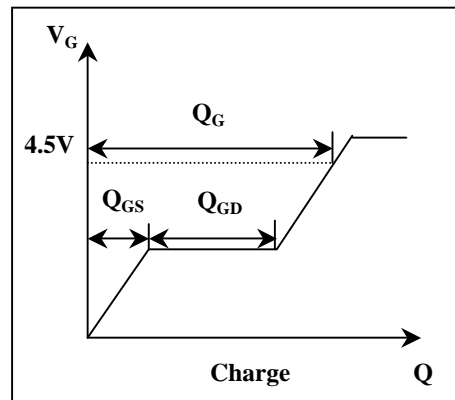


Fig 12. Gate Charge Waveform